




AP 6/28/15

AMENDMENT TRANSMITTAL LETTER				Docket No. M4065.0477/P477	
Application No. 09/939,636-Conf. #4394		Filing Date August 28, 2001		Examiner J. Nguyen	
				Art Unit 2815	
Applicant(s): Kevin M. Devereaux					
Invention: METHOD AND APPARATUS FOR WAFER LEVEL TESTING OF SEMICONDUCTOR USING SACRIFICIAL ON DIE POWER AND GROUND METALIZATION					
TO THE COMMISSIONER FOR PATENTS					
Transmitted herewith is an amendment in the above-identified application.					
The fee has been calculated and is transmitted as shown below.					
CLAIMS AS AMENDED					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	19	- 24 =		x	0.00
Independent Claims	3	- 3 =		x	0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					00.00
<input checked="" type="checkbox"/> Large Entity <input type="checkbox"/> Small Entity					
<input checked="" type="checkbox"/> No additional fee is required for this amendment.					
<input type="checkbox"/> Please charge Deposit Account No. _____ in the amount of \$ _____. A duplicate copy of this sheet is enclosed.					
<input type="checkbox"/> A check in the amount of \$ _____ to cover the filing fee is enclosed.					
<input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.					
<input checked="" type="checkbox"/> The Director is hereby authorized to charge and credit Deposit Account No. <u>04-1073</u> as described below. A duplicate copy of this sheet is enclosed.					
<input checked="" type="checkbox"/> Credit any overpayment.					
<input checked="" type="checkbox"/> Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.					
 Thomas J. D'Amico Attorney Reg. No.: 28,371				Dated: June 4, 2003	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP 2101 L Street NW Washington, DC 20037-1526 (202) 828-2232					

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Docket No.: M4065.0477/P477

(PATENT) 6-10-03

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kevin M. Devereaux

Application No.: 09/939,636

Group Art Unit: 2815

Filed: August 28, 2001

Examiner: J. Nguyen

For: METHOD AND APPARATUS FOR WAFER
LEVEL TESTING OF SEMICONDUCTOR
USING SACRIFICIAL ON DIE POWER
AND GROUND METALIZATION

AMENDMENT UNDER 37 C.F.R. 1.116, REQUEST FOR
RECONSIDERATION AND REQUEST FOR WITHDRAWAL OF FINAL
REJECTION STATUS

Box AF
Commissioner for Patents
Washington, DC 20231

Dear Sir:

In response to the Office Action dated March 4, 2003 (Paper No. 10) finally rejecting claims 1-11 and 25-32, please amend the above-identified U.S. patent application as follows:

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In the Claims

Please rewrite claim 1, 9, 10 and 25 as follows:

1. (Currently Amended) A semiconductor wafer comprising:

at least one first sacrificial conductive line for supplying a first voltage to a plurality of dies fabricated on said wafer;